IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Attorney Docket No. 13912US04)

In the Application of: Ichiro Fujimori	)	***Electronically Filed on 26-FEB-2007***
Serial No. 10/801,260	)	
Filed: March 15, 2004	)	
For: SYSTEM AND METHOD TO REDUCE NOISE IN A SUBSTRATE	)	
Examiner: Phat X. Cao	)	
Group Art Unit: 2814	)	
Confirmation No. 2251	)	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Applicant requests review of the final rejection in the above-identified application, stated in the final Office Action mailed on November 28, 2006 (hereinafter, the FOA) with a period of reply through February 28, 2007. The Applicant also requests review of the arguments stated on pages 2-4 of the Advisory Office Action mailed on February 14, 2007 (hereinafter, the AOA). No amendments are being filed with this request.

This request is being filed with a Notice of Appeal. The review is being requested for the reasons stated on the attached sheets.

REMARKS

The present application includes pending claims 1-15, all of which have been rejected. Claims 1, 8-9, 12, and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Puar, et al., U.S. Patent 6,356,497 (hereinafter, Puar), in view of McCormack, et al., U.S. Patent 6,395,591 (hereinafter, McCormack). Claims 1-10, 12, and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar. Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Puar and McCormack, further in view of Wei, U.S. Patent 6,403,992 (hereinafter, Wei). Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar. The Applicant respectfully submits that the claims define patentable subject matter. The Applicant also respectfully traverses these rejections at least for the reasons stated below.

I. The Examiner's Arguments in the Advisory Office Action (Regarding the Combination of McCormack and Puar)

On pages 2-3 of the AOA, the Examiner states the following (emphasis added):

> [A]t column 4, lines 9-13, McCormack states that:
>
> "A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells. A low P-well resistance has the effect of decoupling the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS process."
>
> From this statement, one of ordinary skill in the art would recognize that the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS shown in Fig. 2 are **prevented by lower the resistance of the lightly doped (p-) substrate 10. The low resistance lightly doped (p-) substrate 10 is provided by placing higher doped (p) layer 12 on top of the lightly doped (p-) substrate 10.**

The Applicant respectfully disagrees with the above assertions by the Examiner. As seen from the underlined citation above, McCormack discloses that **the conventional way to reduce latchup susceptibility is to lower the resistance of the *P-wells*, not the resistance of the *substrate* as suggested by the Examiner. There is absolutely no mention or suggestion in McCormack that latchup susceptibility may be reduced by lowering the resistance of the substrate** "by placing a higher doped layer 12 on top of the lightly doped substrate 10." This is further evidenced by the fact that McCormack's solution for reducing the latchup susceptibility is to use a heavily doped region p++ (14) underneath the p-well (16), and not to reduce the

resistance of the substrate 10. **The Examiner is simply making conclusory statements without any justification whatsoever.**

Therefore, the Applicant maintains the argument stated in Section I (pages 9-13) of the January 22, 2007 response to the FOA. More specifically, the Applicant maintains that neither Puar nor McCormack teach or suggest the limitation of "a shielding layer, wherein said shielding layer reduces transfer of noise in the chip," as recited by the Applicant in independent claim 1. For at least the reasons set forth above, the Applicant respectfully asserts that claim 1 is allowable over McCormack and Puar. The Applicant requests that the rejection of claims 1-15 be withdrawn.

II. The Combination of Puar and McCormack Does Not Disclose "At Least One Transistor of a First Transistor Type That Couples Said Transistor Layer to Said Shielding Layer"

The FOA states the following at page 2 (emphasis added):

> Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; **at least one transistor of a first transistor type (P-type) formed within the well layer;** and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.

The FOA states the following at page 3 (emphasis added):

> Regarding claims 1, 8-9 and 12 , McCormack (Fig. 2) discloses a system for reducing noise in a chip (column 2 , lines 45-50), the system comprising: a substrate layer 10 integrated within the chip ; a transistor well layer 16 /18/22 within the chip, which is isolated or shielded from the substrate layer 10 by a shielding layer 12 ; **a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12,** and the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 22.

The Applicant points out that the full claim 1 limitation, which is not disclosed by McCormack and Puar, is the following: "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer". *See* the Applicant's claim 1. In the above citations, the Examiner has not shown how Puar and McCormack satisfy this claim limitation. **With regard to Puar, the Examiner states the following for support: "at least one transistor of a first**

transistor type (P-type) formed within the well layer," which does not disclose any coupling by Puar of a transistor layer to a shielding layer via a transistor.

With regard to McCormack, the Examiner states the following for support: "a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12," which also does not disclose any coupling of a transistor layer to a shielding layer via a transistor. **However, the transistor 30 of McCormack simply does not have any contact with the layer 12 and there is no coupling by McCormack of a transistor layer to a shielding layer via a transistor.**

III. The Combination of Wei and Puar Does Not Render Claims 1-13 Unpatentable

With regard to the rejection of independent claim 1 under 103(a), the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer," as recited by the Applicant in independent claim 1. The Final Office Action states:

> Wei (Fig . 4) discloses a system for reducing noise in a chip, the system comprising: ... **a transistor G4 of a first transistor type (p type) that couples the transistor layer 46 to the shielding layer 484** ...

See the Final Office Action at page 5 (emphasis added). Furthermore, the Advisory Office Action states the following in page 4:

> Regarding the combination of Wei and Puar, Applicant argues that Wei's Fig. 4 does not disclose "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer" as claimed.
>
> This argument is not persuasive because as clearly stated in the ground of rejection, "at least one transistor of a first transistor" refers to a PMOS transistor (not labeled), "said transistor layer" refers to N-well/P-well layer 46, and "said shielding layer" refers to layer 484. **Clearly, the first transistor type of PMOS couples the transistor layer 46 to the shielding layer 484.**

The Applicant points out that the Examiner's statements listed above, from the FOA and the AOA, are contradictory as the Examiner is using the G4 terminal in the FOA argument, and the PMOS transistor in the AOA argument.

With regard to the above bolded portions of the Examiner's FOA and AOA arguments, the Applicant points out that item G4 designates a ground terminal for the PMOS transistor that is next to the NMOS transistor 46 (note that the PMOS transistor of Wei is not numbered in Figure 4, but it is numbered 52 in

Figure 5). In this regard, G4 of Wei does not designate a "transistor". Furthermore, as illustrated in Figure 4 of Wei, Wei does not disclose or suggest any transistor that couples a transistor layer of any of the PMOS or NMOS 46 with the alleged shielding layer 484. If the Examiner is referring to the PMOS transistor (designated by 52 in Fig. 5 of Wei), the Applicant points out that this argument is still deficient as the PMOS transistor does not couple any transistor layer to a shielding layer. **The PMOS transistor of Wei simply does not have any contact with the alleged shielding layer 484 and there is no coupling by Wei of a transistor layer to a shielding layer via the PMOS transistor.**

Therefore, the Applicant submits that the combination of Wei and Puar does not disclose or suggest at least the limitation of "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer," as recited by the Applicant in independent claim 1. Accordingly, the proposed combination of Wei and Puar does not render independent claim 1 unpatentable, and a prima facie case of obviousness has not been established. The Applicant submits that claims 1-15 are allowable at least for the above reasons.

IV. Conclusion

The Applicant respectfully submits that claims 1-15 of the present application should be in condition for allowance at least for the reasons discussed above and request that the outstanding rejections be reconsidered and withdrawn. The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

/Ognyan I. Beremski/

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